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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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07/13/2000

Dong-Gyu Kim

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HOWREY SIMON ARNOLD & WHITE LLP

BOX 34

1299 PENNSYLVANIA AVENUE NW

WASHINGTON, DC 20004

EXAMINER

RUDE, TIMOTHY L

ART UNIT

PAPER NUMBER

2871

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/615,794

Applicant(s)

KIM, DONG-GYU

Examiner

Timothy L Rude

Art Unit

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-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 11-51 is/are pending in the application.
- 4a) Of the above claim(s) 5-7, 16-18 and 25-51 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 1-4, 9, 11-13, 15 and 20-24 is/are rejected.
- 7) ☐ Claim(s) 8, 14 and 19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claims

1. Claims 1 and 9 are amended.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4, 9, 11-13, 15, and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukada et al (Tsukada) USPAT 4,955,697 in view of Shimada et al (Shimada) USPAT 5,877,830.

As to claims 1-3, Tsukada discloses in Figure 10 his fourth embodiment (col. 8, lines 38-62) a liquid crystal display, comprising:

a first insulating substrate;

a plurality of gate lines, 3, formed at the first substrate to transmit scanning signals;

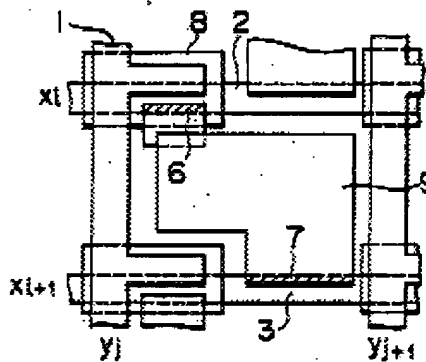
a plurality data lines, 1, crossing over the gate lines to transmit picture signals;

a plurality of pixels defined by the gate lines and data lines, the gate lines dividing the pixel electrode into rows and the data lines dividing the pixel electrodes into columns;

pixel electrodes corresponding to one of the plurality of pixels;

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a second insulating substrate facing the first substrate;
 a liquid crystal layer injected into the gap between said first insulating substrate and said second insulating substrate; and
 a storage capacitor, 7, formed between said pixel electrode and the previous gate line (col. 6, lines 40-48).

FIG. 10

Tsukada does not explicitly disclose a black matrix defining each pixel; wherein an opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer.

Shimada teaches (Title, Abstract, entire patent) a liquid crystal display (LCD) panel comprising:
 a first substrate provided with a plurality of gate, 2, and data, 8, lines, the gate lines being arranged to cross the data lines to define a plurality of pixel regions in a matrix arrangement; a second substrate provided with a black matrix layer (col. 5, lines 50-60) to shield portions other than the pixel regions from light; and liquid crystal layer injected

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between the first and second substrates, wherein the pixel regions in a peripheral portion of the matrix arrangement has an aperture ratio lower than that of the pixel regions in other portions of the matrix arrangement (col. 2, lines 2-12 and col. 6, lines 35-45) in the example where the black matrix overlaps the pixel electrodes, 11 (col. 2, lines 29-42), in areas where no gate or data line exists to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment.

Shimada also teaches in Figure 2 an interlayer insulating film, 9 (Applicant's protective layer) formed over the gate lines and data lines with a plurality of pixel electrodes, 11, formed on said protective layer to allow improved aperture ratio and reduced disclination (col. 7, lines 46-63).

Shimada is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to add an opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment and to allow improved aperture ratio and reduced disclination.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Tsukada with the opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer of Shimada to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment and to allow improved aperture ratio and reduced disclination.

As to claim 4, Shimada, as combined above, teaches formation of the black matrix at the second substrate, both as prior art and as preferred embodiments.

As to claims 9 and 11-12, Tsukada discloses in Figure 10 his fourth embodiment (col. 8, lines 38-62) a liquid crystal display, comprising:
a first insulating substrate;
a plurality of gate lines, 3, formed at the first substrate to transmit scanning signals;

a plurality data lines, 1, crossing over the gate lines to transmit picture signals;

a plurality of pixels defined by the gate lines and data lines, the gate lines dividing the pixel electrode into rows and the data lines dividing the pixel electrodes into columns; a protective layer formed over the gate lines and data lines; a plurality of pixel electrodes, 9, formed on the protective layer, each pixel electrode corresponding to one of the plurality of pixels;

a second insulating substrate facing the first substrate;

a liquid crystal layer injected into the gap between said first insulating substrate and said second insulating substrate; and

a storage capacitor, 7, formed between said pixel electrode and the previous gate line (col. 6, lines 40-48);

a dummy gate line (Applicant's storage capacitor line) formed on said first insulating substrate parallel to the gate line (col. 11, lines 45-68), the storage capacitor line overlapping the pixel electrodes at the first pixel row;

a first storage capacitor formed between said pixel electrode and the previous gate line; and, a second storage capacitor, 7, formed between said pixel electrode and said storage capacitor line;

wherein a gate-off voltage is applied by connecting to the last gate line (col. 11, lines 59-61).

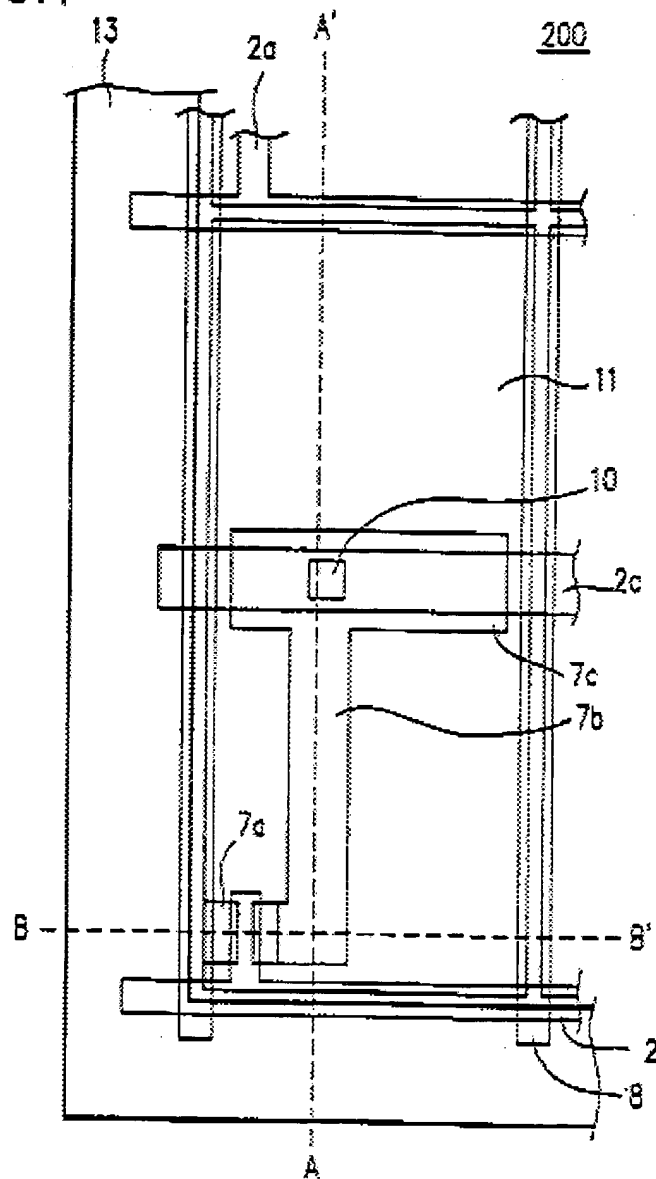
Tsukada does not explicitly disclose a black matrix defining each pixel; wherein an opening ratio of each pixel at the first pixel row is different from the opening ratio of

the pixels at the other pixel rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer.

Shimada teaches (Title, Abstract, entire patent) a liquid crystal display (LCD) panel comprising:

a first substrate provided with a plurality of gate, 2, and data, 8, lines, the gate lines being arranged to cross the data lines to define a plurality of pixel regions in a matrix arrangement; a second substrate provided with a black matrix layer (col. 5, lines 50-60) to shield portions other than the pixel regions from light; and liquid crystal layer injected between the first and second substrates, wherein the pixel regions in a peripheral portion of the matrix arrangement has an aperture ratio lower than that of the pixel regions in other portions of the matrix arrangement (col. 2, lines 2-12 and col. 6, lines 35-45) in the example where the black matrix overlaps the pixel electrodes, 11 (col. 2, lines 29-42), in areas where no gate or data line exists to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment.

FIG. 1



Shimada also teaches in Figure 2 an interlayer insulating film, 9 (Applicant's protective layer) formed over the gate lines and data lines with a plurality of pixel electrodes, 11, formed on said protective layer to allow improved aperture ratio and reduced disclination (col. 7, lines 46-63).

Shimada is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to add an opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment and to allow improved aperture ratio and reduced disclination.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Tsukada with the opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows and a protective layer formed over the gate lines and data lines with a plurality of pixel electrodes formed on said protective layer of Shimada to prevent light leaks in areas where no gate or data line exists despite mating substrate misalignment and to allow improved aperture ratio and reduced disclination.

As to claims 13 and 15, Shimada, as combined above, teaches formation of the black matrix at the second substrate, both as prior art and as preferred embodiments.

As to claims 20-22, Tsukada discloses connection of the storage capacitor line to the last gate line (col. 11, lines 59-61) (Applicant's further comprising a gate-off line formed on said first substrate to transmit a gate-off voltage, wherein the gate-off line and said storage capacitor line are formed at the same layer as the gate line, wherein

the gate-off line and said storage capacitor line are electrically connected to each other via a connection member, and the connection member is formed at the same layer as the data line or said pixel electrode).

As to claims 23 and 24, Tsukada discloses a functional liquid crystal display with driving circuitry and voltage driving scheme (col. 11, lines 61-66) (Applicant's further comprising gate signal transmission films arranged at said first substrate and provided with a gate driving integrated circuit that is electrically connected to the gate lines and outputs gate driving signals, and data signal transmission films arranged at said first substrate and provided with a data driving integrated circuit that is electrically connected to the data lines and outputs data driving signals, wherein a common electrode wire for applying the common electrode voltage (V_{com}), a gate-on wire for applying the on-voltage V_{on} to the TFTs controlling the picture signals, a gate-off wire for applying the off-voltage V_{off} , and wires for transmitting carry-in or gate-clock signals are formed on the edge portion of the first substrate between the gate signal transmission film and the data signal transmission film, wherein the common electrode wire, the gate-on wire, and the gate-off wire at the same layer as the gate lines with the same material).

Allowable Subject Matter

3. Claims 8, 14, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

As to claim 8, relevant prior art of record did not disclose, alone or in combination, the liquid crystal display of claim 2, wherein the opening ratio of the first pixel row is designed to be *60-80% of the opening ratio* of the other pixel rows. The closest combination is Tsukada in view of Shimada, but they do not explicitly disclose the claimed range of *60-80%*.

As to claim 14, relevant prior art of record did not disclose, alone or in combination, the liquid crystal display of claim 13, wherein opening width of said black matrix at the first pixel row in the *longitudinal direction of the gate line is identical to* opening width of said black matrix at the other pixel rows. The closest combination is Tsukada in view of Shimada, but they do not explicitly disclose an opening width of said black matrix at the first pixel row in the longitudinal direction of the gate line is identical to opening width of said black matrix at the other pixel rows.

As to claim 19, relevant prior art of record did not disclose, alone or in combination, the liquid crystal display of claim 11, wherein the opening ratio of the first pixel row is designed to be *60-80% of the opening ratio* of the other pixel rows. The closest combination is Tsukada in view of Shimada, but they do not explicitly disclose the claimed range of 60-80%.

Response to Arguments

4. Applicant's arguments with respect to claims 1-4, 9, 11-13, 15, and 20-24 have been considered but are moot in view of the new ground(s) of rejection.

References cited but not applied are relevant to the instant Application.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy L Rude whose telephone number is (703) 305-0418. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H Kim can be reached on (703) 305-3492. The fax phone numbers

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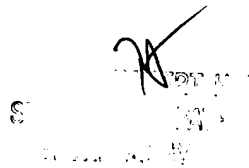
for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4900.



Timothy L Rude
Examiner
Art Unit 2871

TLR
January 20, 2004



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